虹美功率半导体
www.hmpowersemi.com

# KP5635G

## N-Channel 20V (D-S) MOSFET

## GENERAL DESCRIPTION

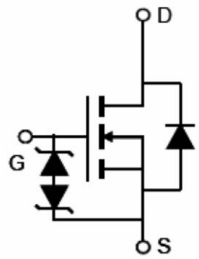
The HM2302D is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

## FEATURES

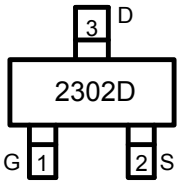
- $R_{DS(ON)}$= 270 mΩ @$V_{GS}$=4.5V
- $R_{DS(ON)}$= 330 mΩ @$V_{GS}$=2.5V
- $R_{DS(ON)}$= 450 mΩ @$V_{GS}$=1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding

## APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch




N-Channel




Marking and pin Assignment


SOT-23 top view

## Absolute Maximum Ratings ($T_A$=25℃ Unless Otherwise Noted)

| Parameter | Symbol | Maximum Ratings | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 20 | V |
| Gate-Source Voltage | $V_{GS}$ | ±8 | V |

# KP5635G

**N-Channel 20V (D-S) MOSFET**

## Absolute Maximum Ratings ($T_A$=25℃ Unless Otherwise Noted)

| Parameter | Symbol | Maximum Ratings | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 20 | V |
| Gate-Source Voltage | $V_{GS}$ | ±8 | V |

## Electrical Characteristics ($T_j$ =25℃ Unless Otherwise Specified)

| Symbol | Parameter | Limit | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **STATIC** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_D$=250μA | 20 | | | V |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=250μA | 0.45 | | 1.2 | V |
| $I_{GSS}$ | Gate Leakage Current | $V_{DS}$=0V, $V_{GS}$=±8V | | | ±10 | μA |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=20V, $V_{GS}$=0V | | | 1 | μA |
| $R_{DS(ON)}$ | Drain-Source On-Resistance[a] | $V_{GS}$=4.5V, $I_D$=890mA | | 220 | 270 | mΩ |
| | | $V_{GS}$=2.5V, $I_D$=780mA | | 260 | 330 | |
| | | $V_{GS}$=1.8V, $I_D$=700mA | | 330 | 450 | |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=350mA, $V_{GS}$=0V | | 0.75 | 1.2 | V |
| **DYNAMIC** | | | | | | |
| Ciss | Input Capacitance | $V_{DS}$=15V, $V_{GS}$=0V, f=1MHZ | | 21 | | pF |
| Coss | Output Capacitance | | | 15 | | |
| Crss | Reverse Transfer Capacitance | | | 8 | | |
| Qg | Total Gate Charge | $V_{DS}$=25V, $V_{GS}$=10V, $I_D$=0.22A | | 6.7 | | nC |
| Qgs | Gate-Source Charge | | | 1.2 | | |
| Qgd | Gate-Drain Charge | | | 0.9 | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$=10V, $R_L$ =3Ω<br>$V_{GEN}$=10V,$R_G$=10Ω | | 120 | | ns |
| tr | Turn-On Rise Time | | | 317 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 748 | | |
| $t_f$ | Turn-Off Fall Time | | | 716 | | |

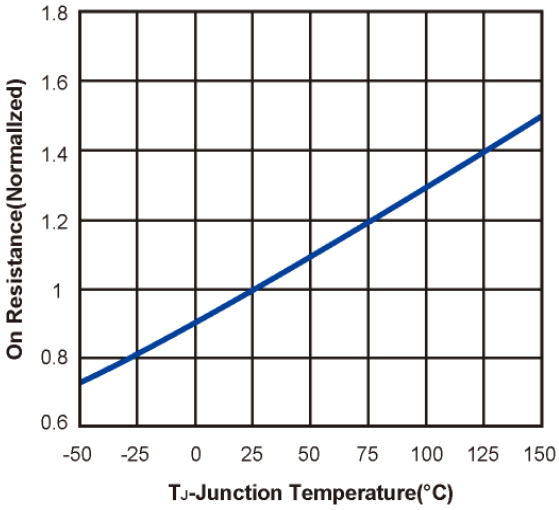
Notes: a. Based on epoxy or solder paste and bond wire Cu wire 1mil×1(S), Cu wire 1mil×1(G) on each die of SOT-523 package.

b. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%.

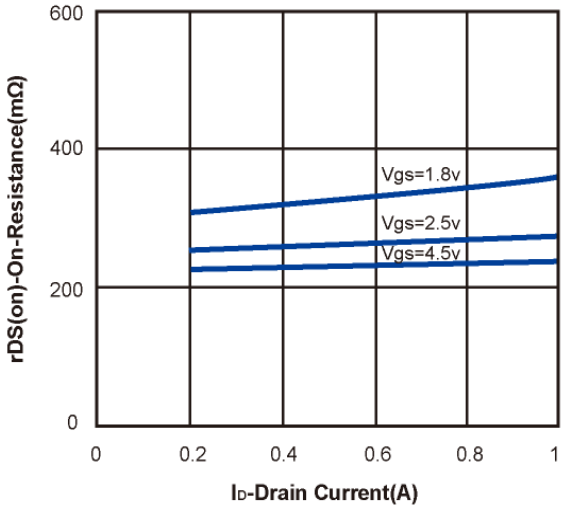
c. Force mos reserves the right to improve product design, functions and reliability without notice.

## Typical Characteristics ($T_J$ =25℃ Noted)

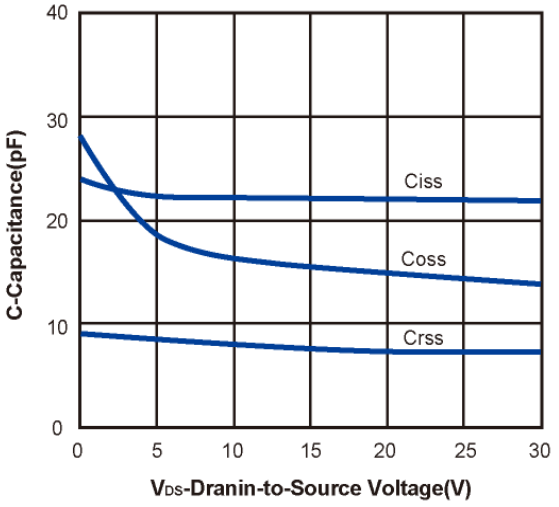
On Resistance vs. Junction Temperature



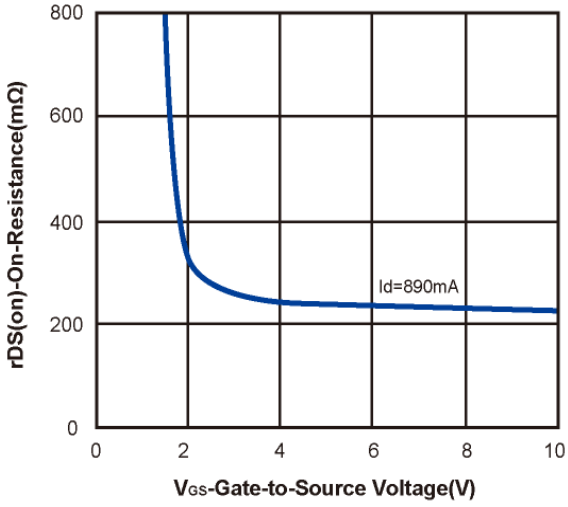

On Resistance vs. Drain Current



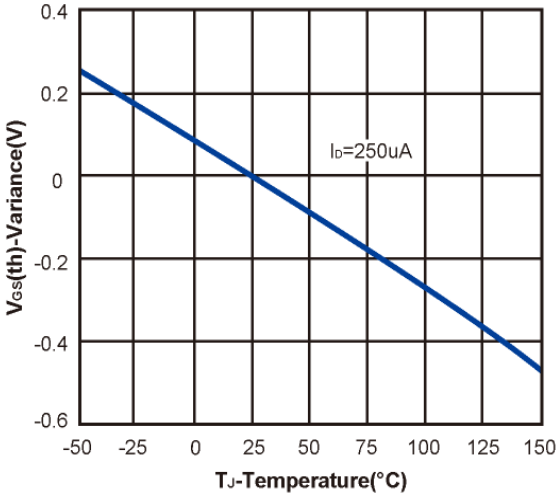

Capacitance



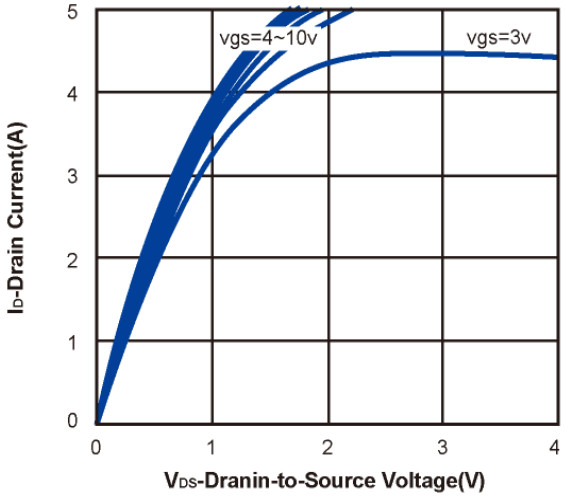

On Resistance vs. Gate-to-Source Voltage



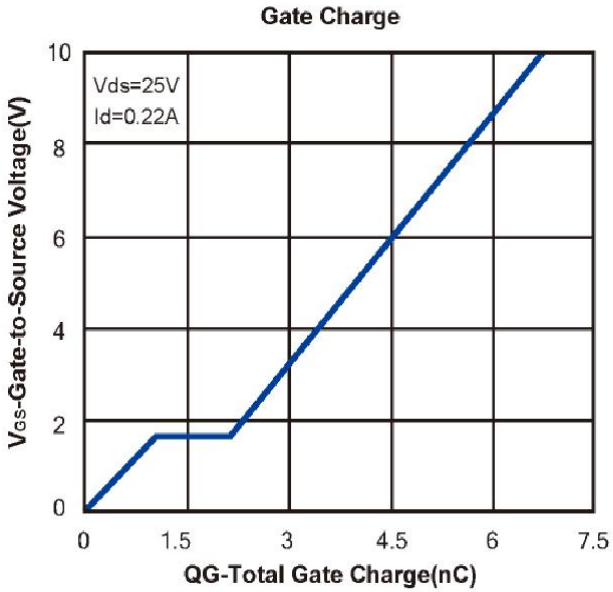

Threshold Voltage

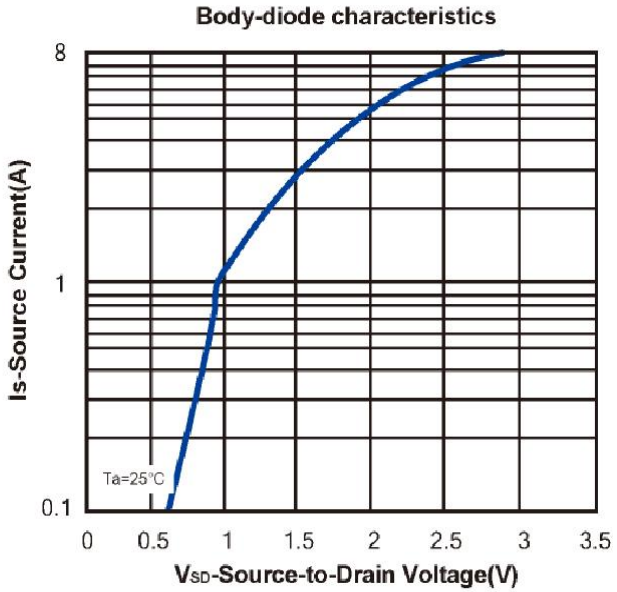



On-Region Characteristics



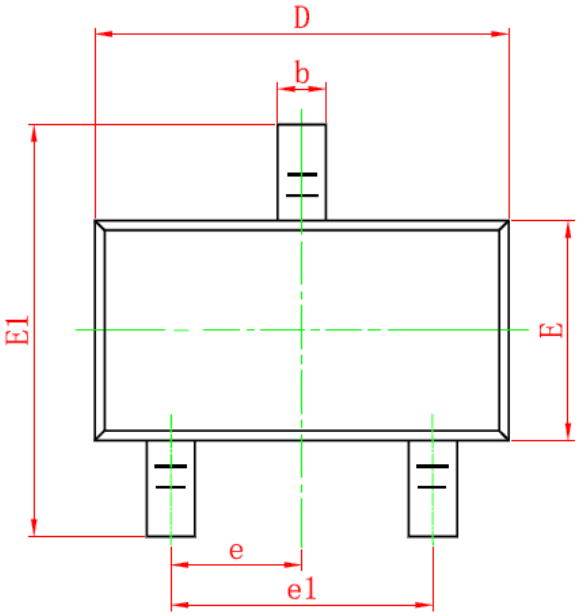
## Typical Characteristics ($T_J$ =25℃ Noted)

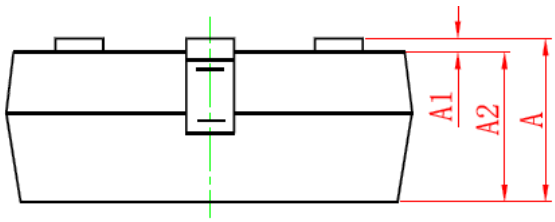


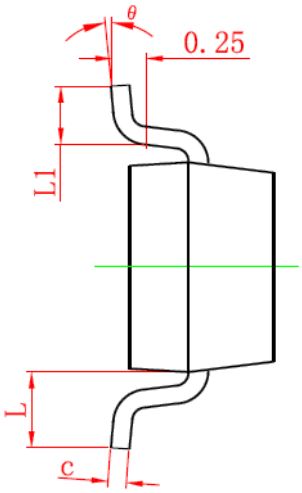



# SOT-23 PACKAGE INFORMATION

Dimensions in Millimeters (UNIT:mm)




| Symbol | Dimensions in Millimeters | |
|---|---|---|
| | MIN. | MAX. |
| A | 0.900 | 1.150 |
| A1 | 0.000 | 0.100 |
| A2 | 0.900 | 1.050 |
| b | 0.300 | 0.500 |
| c | 0.080 | 0.150 |
| D | 2.800 | 3.000 |
| E | 1.200 | 1.400 |
| E1 | 2.250 | 2.550 |
| e | 0.950TYP | |
| e1 | 1.800 | 2.000 |
| L | 0.550REF | |
| L1 | 0.300 | 0.500 |
| θ | 0° | 8° |

## NOTES

1. All dimensions are in millimeters.
2. Tolerance ±0.10mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.